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VRQED Inc - IEEE Micro, 1732 - doi.ieeeecs.org

... Figure 3. The 21164 **instruction pipeline**, which executes in seven integer, nine floating ... Replay traps occur in the following cases: correctable **ECC** error from ...

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CF Webb, JS Liptay - IBM J RES DEV, 1997 - doi.ieeeecs.org

... These DWs have **ECC** applied, are saved in the store buffer, and are sent to the La-cache after the storing instruction has completed ... 7. **Instruction pipeline** ...

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JH Hesson, J LeBlanc, SJ Ciavaglia, WT Esling, PA ... - US Patent 5,625,789, 1997 - Google Patents

... correcting codes (**ECC**) or byte parity information. ... that are being written back to the register file 17 during the last stage of an **instruction pipeline** stage. ...

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TJ Siegel, RM Averill III, MA Check, BC Giamei, BW ... - Micro, IEEE, 1999 - ieeexplore.ieee.org

... cache **ECC** generation on results in R unit R unit cross- checks duplicate E unit data Write results to R unit Figure 3. I unit and E unit **instruction pipeline**. ...

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[Multiple instruction issue in the NonStop cyclone processor - all 3 versions »](#)

RW Horst, RL Harris, RL Jardine - ACM SIGARCH Computer Architecture News, 1990 - portal.acm.org

... If the next two instructions are pairable, they are both moved into rank 1 of the **instruction pipeline**, and the ... I ! 32MB or 64 MB I - **ECC** Memory ...; . i ...

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RE Kessler - Micro, IEEE, 1999 - ieeexplore.ieee.org

... **Instruction pipeline**—Fetch The **instruction pipeline** begins with the fetch stage, which delivers four instructions to the out-of-order execution engine each ...

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[HAVING AN INSTRUCTION PIPELINE FOR CONCURRENTLY PROCESSING A PLURALITY OF INSTRUCTIONS](#)

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... [54] HAVING AN **INSTRUCTION PIPELINE** FOR CONCURRENTLY PROCESSING A PLURALITY OF INSTRUCTIONS [75] Inventor: E. Leon Willette, San Jose, Calif. ... A/T 4 ecc CD ...

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[Apparatus to dynamically control the out-of-order execution of load-store instructions in a ... - all 2 versions »](#)

JH Hesson, J LeBlanc, SJ Ciavaglia - US Patent 5,615,350, 1997 - Google Patents

... The data and **ECC** are buffered by data cache (DCACHE) fill buffer ... operation is now described as a store instruction proceeds through the **instruction pipeline**. ...

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MJK Nielsen - Compcon Spring'91. Digest of Papers - ieeexplore.ieee.org

... 1-Mbit-DRAM mem- ory modules, or up to 480 MBytes of **ECC** memory using 4 ... RD ALU ME WB j JE JMEI4 WB IF RDIALUMEPWBI Figure 2 R3000 **Instruction Pipeline** The high ...

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[Apparatus to perform source operand dependency analysis perform register renaming and provide rapid ... - all 3 versions »](#)

JH Hesson, J LeBlanc, SJ Ciavaglia, WT Esling, PA ... - US Patent 5,884,061, 1999 - Google Patents

... shown) to receive and transmit address and control codes and to receive and transmit data and error correcting codes (ECC) or byte ... 15 instruction pipeline stage ...
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